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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dureseti Chidambarao

Group Art Unit:2822

Patent No: 6,887,751 B2

Examiner: Perkins, Pamela E

Filed: September 12, 2003

For: **MOSFET PERFROMANCE IMPROVEMENT USING DEFORMATION IN SOI  
STRUCTURE**

**COMPLETION OF RECORD**

Commissioner for Patents  
U.S. Patent and Trademark Office  
Customer Service Window  
Randolph Building  
401 Dulany Street  
Alexandria VA 22314

Sir :

For the possible benefit of anyone subsequently evaluating the scope and/or validity of the above patent, it is requested that the following reference, copy enclosed, be placed in the file wrapper.

US Patent No. :6,831,292 B2.

This reference was recently found by the Applicant. The undersigned has not reviewed the teachings of this reference in detail and thus makes no representation concerning their relevancy or materiality.

Respectfully submitted,  
Dureseti Chidambarao

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August 15, 2005  
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